METHOD AND SYSTEM FOR REDUCING TEST DATA VOLUME IN THE TESTING OF LOGIC PRODUCTS

ABSTRACT OF THE DISCLOSURE

A method and system for reducing test data volume in the testing of logic products such as integrated circuit chips. Test data loaded by a tester into the logic product to apply to portions of combinational logic circuitry therein in order to detect faults comprises "care" bits and "non-care" bits. The care bits target focal faults of interest in the logic circuitry being tested while the non-care bits do not. According to the invention, non-care bits in the test vector data are filled with repetitive background data to provide for a high degree of compressibility of the test vector data. A substantial portion of the care bits may also be set to a repetitive value and the original values later recovered.